BEST AVAILABLE COPY

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 January 2005 (27.01.2005)

PCT

(10) International Publication Number
WO 2005/008695 A2

(51) International Patent Classification[7]: H01F 17/00

(21) International Application Number: PCT/IB2004/051234

(22) International Filing Date: 15 July 2004 (15.07.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
03102261.9 23 July 2003 (23.07.2003) EP

(71) Applicant *(for all designated States except US)*: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: DETCHEVERRY, Celine, J. [FR/BE]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). VAN NOORT, Wibo, D. [NL/BE]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

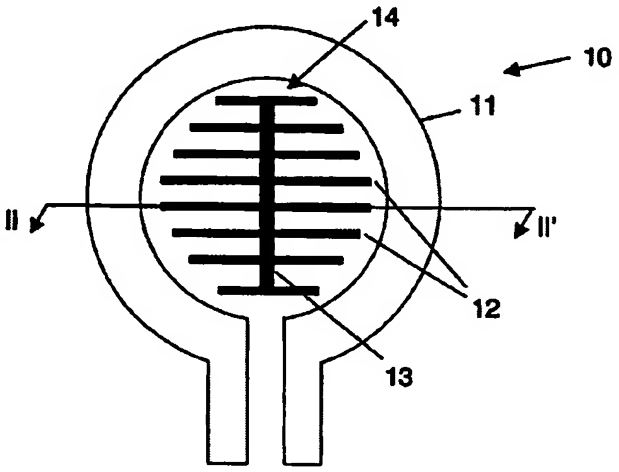
(74) Agent: ELEVELD, Koop, J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

*[Continued on next page]*

(54) Title: INDUCTIVE AND CAPACITIVE ELEMENTS FOR SEMICONDUCTOR TECHNOLOGIES WITH MINIMUM PATTERN DENSITY REQUIREMENTS




(57) Abstract: The present invention provides a semiconductor device comprising a plurality of layers, the semiconductor device comprising: - a substrate having a first major surface, - an inductive element fabricated on the first major surface of the substrate, the inductive element comprising at least one conductive line, and - a plurality of tilling structures in at least one layer, wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element. It is an advantage of the above semiconductor device that, by using such tilling structures, an inductive element with improved quality factor is obtained. The present invention also provides a method for providing an inductive element in a semiconductor device comprising a plurality of layers.

WO 2005/008695 A2